Drawing Amendments

As described on page 14, lines 21-29, the several bits comprising each bit-wise code are referred to as "BCBx", whereas, in Figs. 5A and 5B, these bits are incorrectly referenced as "CCBSx". This drafting error has been corrected in the replacement Figs. 5A and 5B, submitted herewith. Entry of the correct drawing is respectfully requested.

Remarks

In the Action:

1. Claim 27 was objected to under 37 CFR 1.75(c), and claims 25 and 26 were conditionally objected to under 37 CFR 1.75. In response, Applicants have amended claim 27 to make it independent of claim 24. In claim 24, each of the "parity bits [is] related to all m bits stored in respective one of said columns". In contrast, in claim 27, each of the "check bits [is] related to a unique combination of at least two of said bits stored in a respective one of said columns". In view of these substantive distinctions, Applicants respectfully submit that the subject matter of claim 27 (and dependent claims 28-30) is more than sufficiently distinct from the subject matter of claim 24 (and dependent claims 25-26) for the purposes of 37 CFR 1.75(c). Reconsideration and withdrawal of this objection are respectfully requested.

2. Claims 24-25, 27-28 and 31-35 were rejected under 35 U.S.C. § 102 (e) as being anticipated by McGinn, US 6,216,251 ("McGinn"). In McGinn, "the parity generation operation occurs after every memory write operation." (See, McGinn, col. 6, lines 3-5.) During each parity generation operation, re-calculation of the "column parity vector" requires the "parity controller [to access] the entire [memory] array". (See, McGinn, col. 6, lines 31-32.) Thus, in McGinn, every memory write operation requires the parity generation controller to read each and every word in the memory array. In contrast, in Applicants' system, a write operation to a selected address requires reading of only the single word stored at the selected address, comparison of the "old" stored word to the "new" word to be stored, and, then, the updating of the parity (or check) bits based on the results of that comparison. (See, specification, p. 11, lines 8-12; and Fig. 11 as described on p. 16, lines 5-28.) The dramatic reduction in effective write cycle time and resultant significant improvement in throughput of the Applicants' system over the McGinn system are quite clear. In order to reflect this distinct difference in functionality, Applicants have amended claim 24. In addition to making claim 27 independent, Applicants have also amended claim 27 to reflect this distinct difference in functionality. Reconsideration and withdrawal of the rejection of claims 24-25 and 27-28 are respectfully requested.

With respect to the rejection of claims 31-35, Applicants wish to point out that nothing in McGinn suggests that the methods (or circuits) disclosed therein are applicable to an "ordered string", and, in particular, to an "ordered string" received "in any order". (Claim 31, line 4.) Further, in McGinn, the simple row/column parity generation circuit generates each row/column parity bit based on all of the bits comprising a respective row/column, whereas claim 31 requires the "parity generation circuit [to generate] a plurality of parity bits, each related to a unique combination of said bits". (Claim 31, lines 5-6.) Assuming, *arguendo*, that the simple parity generation circuit of McGinn is replaced by a more robust parity generation circuit such as a conventional "single error correction, double error detection" ("SECDED") circuit (as discussed in Carson, below), the combination still fails to satisfy all limitations of claim 31 since a conventional SECDED circuit must receive all bits in a pre-determined sequence (otherwise it lacks sufficient information to determine which parity/check bits will be affected by which data bits). Thus, the subject matter of claim 31 is

patentably distinct over McGinn for the purposes of 35 U.S.C. § 102 (e). In this regard, Applicants wish to note that MPEP § 2131 provides:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. v Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053, (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claims.

Since, as seen above, "each and every element as set forth the claim[s]" are not "found, either expressly or inherently described in a single prior art reference", the rejection of claims 31-35 under 35 U.S.C. 102 (e), based on McGinn, is not well founded and should be withdrawn.

3. Claims 26, 29 and 30 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over McGinn. In view of the amendment of claims 24 and 27, as set forth above, reconsideration and withdrawal of the rejection of claims 26, 29 and 30 are respectfully requested.

4. Claims 1-9 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Peterson *et al.*, US 6,598,197 ("Peterson"). In response, Applicants have cancelled claims 1-5 and amended claim 6 to incorporate, in independent form, the subject matter of claim 10. Accordingly, claims 6-9 and 11-13 (as amended herein to depend from now-independent claim 6) should now be allowable.

5. Claims 14-15 and 17-23 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Carson *et al.*, US 5,432,729 ("Carson") in view of McGinn. In Carson, only classic row/word-wise EDACs are disclosed. In McGinn, a combination row/word-wise and column/bit-wise parity generation circuit (forming a single plane EDAC) is disclosed. In neither, however, is there any teaching or suggestion of "a stack error detection circuit to detect an error in a bit of a stack of ... bits [each in a respective one of a plurality of planes of rows and columns". (Claim 14, lines 15-16, in view of lines 2-4.) Without so much as a suggestion in the cited references as to such functionality, the rejection of claims 14-15 and 17-23 under 35 U.S.C. § 103 (a) is unsupported and should be withdrawn.

Applicants have added new claims 36 (dependent on amended claim 24) and 37 (dependent on amended claim 27) to add subject matter believed to be fully disclosed in the application as filed. In particular, Applicants would direct the Examiner's attention to page 11, lines 13-20, and page 17, lines 11-13 (as illustrated at step 80 in Fig. 8A). Allowance of new claims 36 and 37 is respectfully requested.

Applicants respectfully request entry of the amendments proposed hereinabove, and submit that claims 6-9, 11-15 and 17-37, as may be amended herein, are allowable. In the belief that we have responded to each and every rejection contained in the Action, Applicants respectfully request the reconsideration and allowance of claims 6-9, 11-15 and 17-37.

Respectfully submitted,

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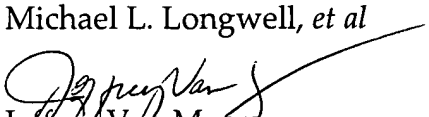

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